Amendments to the Claims

1.-72. (Canceled)

73. (Original) A system comprising:

a bit extractor; and

a remainder value generator coupled to the bit extractor, wherein the bit extractor is configured to extract a residuary subset bitfield associated with an intermediate remainder calculating value and a compound exponent value, and wherein the remainder value generator is configured to generate a remainder value that is associated with the intermediate remainder calculating value.

74. (Original) A system as defined in claim 73, wherein the residuary subset bitfield is associated with an upper-boundary bit position value and a lower-boundary bit position value, and wherein the compound exponent value includes the upper-boundary bit position value and the lower-boundary bit position value.

75. (Previously Presented) A system as defined in claim 73, wherein the remainder value generator is configured to generate the remainder value using at least one of an addition operation, a multiplication operation or a bit-shift operation.

76. (Original) A system as defined in claim 73, wherein the remainder value generator is configured to generate a remainder value equal to zero if the intermediate remainder calculating value equals zero.

77. (Original) A system as defined in claim 73, wherein the remainder value generator is configured to locate the remainder value stored within a data structure location associated with the intermediate remainder calculating value.